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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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extols

Applicant(s): T. SAITO et al
Serial No.: 09/850,162
Filed: May 8, 2001
For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
AND A METHOD OF MANUFACTURING THE SAME
Group: 2812
Examiner: R. E. POMPEY

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SUBMISSION UNDER 37 CFR §1.56

MS: ISSUE FEE

Commissioner For Patents
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Sept. 30, 2003
(Tuesday)

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Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of three (3) art documents (including two (2) U.S. Patents and a published European Patent Application [in the English language]) that were uncovered by applicants in order to complete the record and in keeping with duty of disclosure/candor requirements. Also enclosed herewith is a listing of these documents in equivalent form PTO-1449, as a convenience to the Examiner.

Applicants submit, the disclosures/teachings associated with these three (3) art documents would not have led to the key aspects of claimed invention of the present application such as noted in the supportive discussion/rebuttal arguments submitted in the responsive amendment of September 29, 2003. In that regard, the following comments are being submitted by applicants with regard to each of these art documents.

I. Zhao et al (US 6,037,664)

Zhao et al disclosed a dual damascene interconnect scheme for a multiple metallization structure. Zhao et al disclosed a scheme in which the encapsulation layers such as 33 and 34 in Fig. 16 are formed by selectively depositing the conductors on conductive layers 10 and 29, respectively. Zhao et al's scheme, it is submitted, did not call for cleaning steps to occur before and after the formation of the encapsulation layers 33 and 34 of Zhao et al's structure. Such cleaning steps in addition to other featured aspects thereof, it is submitted, are featured in the present invention.

II. Joshi et al (US 5,976,975)

Joshi et al disclosed a tungsten (W) refractory metal (e.g., 17) deposited by a CVD method and which is planarized by a CMP (chemical-mechanical polishing) or RIE (reactive ion etching) process on a copper metallization (e.g., 16). It is submitted, however, Joshi et al did not disclose nor suggest forming the tungsten refractory metal 17 by a selective growth process, as is required in connection with the formation of the cap conductive layer of the present invention. (Column 7, lines 10-37, and Figs. 2d-2e, in Joshi et al.)

III. EP 0 949 673 A2 (Clevenger et al)

This document discloses a damascene interconnect structure. The method disclosed calls for liner layers (e.g., 139, in Fig. 1D, 159 in Fig. 1I and 239 in Fig. 2E) to be deposited by a CVD method and planarized by a CMP process on a conductor layer (e.g., 140, 160 and 260). For example, the liner layer 139 is deposited on the surface 131, thereby filling the recess (see Fig. 1D). As can be seen from Fig. 1E, the liner 139 is polished by a CMP process to planarize the surface which produces a

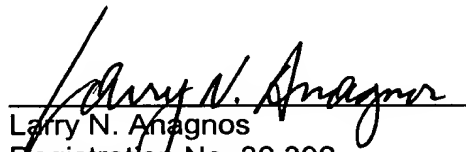
contact 140 that is encapsulated by liner 142. (Page 4, lines 42-45, in Clevenger et al.) It is submitted, however, this document, also, is deficient at least insofar as failing to disclose or suggest forming such liners as 139, 159 and 239 through using a selective growth technique such as that called for by the claimed disclosure of the present application.

For at least the reasons noted above, the present claimed subject matter, applicants submit, is considered patentable thereover. Nonetheless, applicants are making known these uncovered art documents for purposes of completing the record and in keeping with any duty of disclosure/candor requirements pertaining thereto.

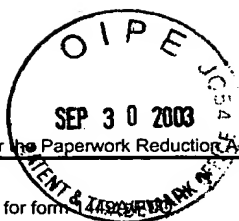
Acceptance and formal entry therefor of this submission is respectfully requested.

If any costs are due in accordance with the filing of this paper, please charge same to the account of Antonelli, Terry, Stout & Kraus, LLP, Account No. 01-2135 (501.39868X00) and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP


Larry N. Anagnos
Registration No. 32,392

LNA:dks
(703) 312-6600



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known	
		Application Number	09/850,162
		Filing Date	May 8, 2001
		First Named Inventor	SAITO, T. et al
		Art Unit	2812
		Examiner Name	R. POMPEY
Sheet 1 of 1	Attorney Docket Number	501.39868X00	

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-6,037,664		03-14-2000	ZHAO et al	
		US-5,976,975		11-02-1999	Joshi et al	
		US-				
		US-				
		US-				
		US-				
		US-				
		US-				

FOREIGN PATENT DOCUMENTS							
Examiner Initials ¹	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					
		EP 0949673 A2		10-13-1999	Clevenger et al		

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard St.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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